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Many-Valued Gates for Reducing the Chip-Area of Integrated Circuits

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Abstract. In this paper are proposed new many-valued gates ***K-PLA***, ***T(2/K)*** and ***T(K/2)*** for a logical synthesis of digital integrated circuits. The semi-custom integrated circuit ***K-PLA*** has the architecture of a Programmable Logic Array of a type ***AND-OR*** and includes new ***K***-valued valves ***MAX***, ***MIN*** and ***GATE(A,j)***. A gate ***T(2/K)*** (***T(K/2)***) is intended for transformation binary (***K***-valued) entrance words into ***K***-valued (binary) output words. The method of the logical synthesis with the use ***K-PLA***, ***T(2/K)*** and ***T(K/2)*** allows to reduce nearly three times the chip-area, which is essential for placing of the circuit's realization of the system of partial Boolean functions .

Keywords: Programmable Logic Array, logical synthesis, semi-custom integrated circuit, many-valued gate, reducing of chip-area.

In this paper we look at the relevant problem of minimization of a chip-area of integrated circuits.

This paper is the obligatory supplement of our article [7], where are absent figures for explanation of functioning new many-valued gates.

The work done in this area includes the Dagon [1], MIS [2,3] and Ceres [4] systems. Results [5] and [6] were received with the help of the library basis of gates. For example, the paper [5] communicates about gate "AND/OR/NAND/NOR constraint".

Our method of the synthesis of circuits [7] allows to sinthesize integrated circuits with new many-valued gates ***K-PLA***, ***T(2/K)*** and ***T(K/2).*** The input information for synthesis is a system of partial Boolean functions ***(m,r,q)***. For example, we sinthesize the system ***(18,6,20)***, showed on Fig.1.

There are main stages of our method of logical synthesis of integrated circuits [7].

1.The choice of the quantity of K for gates in a circuit's realization of the system of partial Boolean functions (m,r,q). We take that K, where $\log_2 K = [\log_2 K]$.

2. The coding the binary input and output words of (m,r,q) by K-valued words with length $n =]m/\log_2 K[$ and $s =]r/\log_2 K[$.

In this stage we construct the system of partial many-valued logical functions (n,s,q), which corresponds to system (m,r,q). For our system $(18,6,20)$, showed on Fig. 1, we get the system $(6,2,20)$, showed on Fig. 2.

x1 x18	g1 g6
100 011 000 110 011 100	011100
100 010 111 100 100 101	110110
111 101 100 011 010 010	010011
000 100 100 011 100 111	000110
101 100 101 011 000 101	101101
100 011 100 110 010 011	010001
000 010 110 100 111 001	010101
100 110 001 101 110 000	101101
000 110 100 111 001 001	110110
111 110 001 000 110 101	111111
100 010 110 111 010 010	000101
100 011 100 110 110 100	011101
000 110 001 101 001 011	110100
100 011 100 001 100 111	000001
111 000 110 110 000 111	011011
111 011 000 110 110 100	111111
100 011 100 111 001 001	100100
001 001 110 010 000 111	111011
100 111 001 001 000 111	110001
101 100 100 111 000 110	011010

Fig. 1.

v1 v6	f1 f2
4 3 0 6 3 4	3 4
4 2 7 4 4 5	6 6
7 5 4 3 2 2	2 3
0 4 4 3 4 7	0 6
5 4 5 3 0 5	5 5
4 3 4 6 2 3	2 1
0 2 6 4 7 1	2 5
4 6 1 5 6 0	5 5
0 6 4 7 1 1	6 6
7 6 1 0 6 5	7 7
4 2 6 7 2 2	0 5
4 3 4 6 6 4	3 5
0 6 1 5 1 3	6 4
4 3 4 1 4 7	0 1
7 0 6 6 0 7	3 3
7 3 0 6 6 4	7 7
4 3 4 7 1 1	4 4
1 1 6 2 0 7	7 3
4 7 1 1 0 7	6 1
5 4 4 7 0 6	3 2

Fig. 2.

Fig. 1. System of partial Boolean funtions $(18,6,20)$
Fig. 2. System $(6,2,20)$ of partial 8-valued logical functions

3. The construction of the circuit S with $T(2/K)$, K-PLA and $T(K/2)$ for realization (m,r,q). The circuit S is showed on Fig. 3.

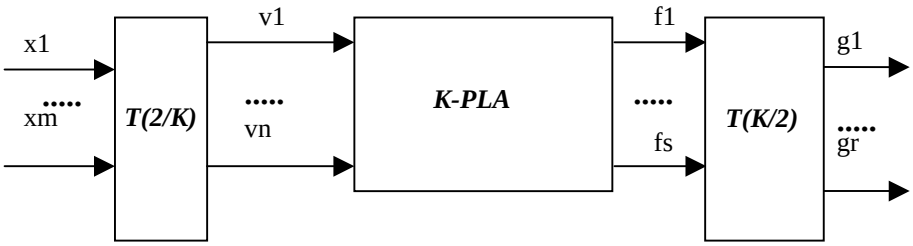

Fig. 3. Circuit ***S*** for synthesis of ***(m,r,q)***

4. The minimization of the system of partial ***K***-valued logical functions ***(n,s,q)***.

With that aim we generate system-intervals which realize by implicants and construct SOP-system in basis $\{\vee, \wedge, v_i^j, 1,2, ...,K-1\}$.

5. The creation the special matrixes for realization of the concrete parameters of gates for ***K-PLA*** with the help of the ***K-PLA*** – programmer.

6. The completion of the synthesis with the help of the ***K-PLA*** – programmer.

It is easy to explain structures of all blocs showed on Fig. 3 with the help of the concrete examples.

Fig. 4 shows the structure of translator ***T(2/K)*** for three input pins and ***K=8,*** where

○ is the gate ***NOT***, △ is the gate ***AND***, ▼ is the gate for realization of operation ***Max***, □ is the gate ***GATE(A,j)***.

The gate ***GATE(A,j)*** has one input pin and one output pin, where $y = A$ for $x=j$ and $y = 0$ for $x \neq j$. The main parameters ***A*** and ***j*** for ***GATE(A,j)*** we must be able to modify with the help of a special equipment called by programmer (similar as PROM blower).

If input signals of ***T(2/K)*** are equal to ***xi1 = 1, xi2 = 0, xi3 = 1,*** to input signal of ***GATE(5,1)*** is equal to 1 and it's output signal is equal to 5. Then the output signal of ***T(2/K)*** is equal to 5 also.

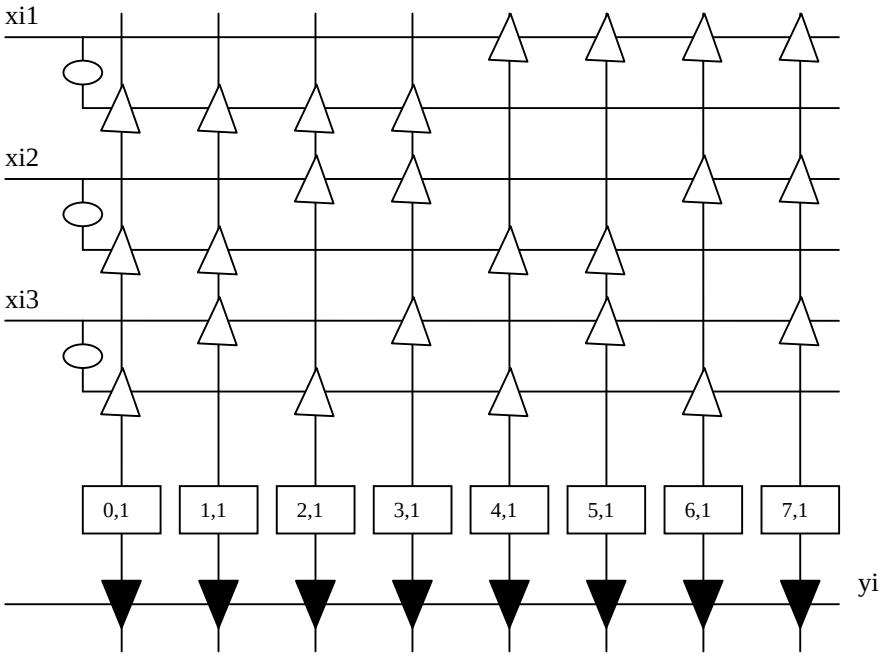

Fig. 4. Structure of translator ***T(2/K)*** for three input pins

Fig. 5 shows the structure of translator ***T(K/2)*** for one input pin, three output pins and ***K=8,*** where ▽ is the gate ***OR,*** □ is the gate ***GATE(A,j)***.

For example, if input signal of ***T(8/2)*** is equal to ***fi = 4,*** input signal of the gate ***GATE(1,4)*** is equal to 4 so and output signal of the gate ***GATE(1,4)*** is equal to 1. Then output signals of ***T(2/K)*** are equal to ***gi1 =1, gi2 = 0, gi3 = 0.***

Figure 6 shows the structure of ***K-PLA(6,2,20)*** for ***K=8*** with 6 input pins, 2 output pins and 20 intermediate lines. This block includes gates ***MIN, MAX, GATE(7,j), GATE(A,7),*** which are described as ▲, ▼, and □.

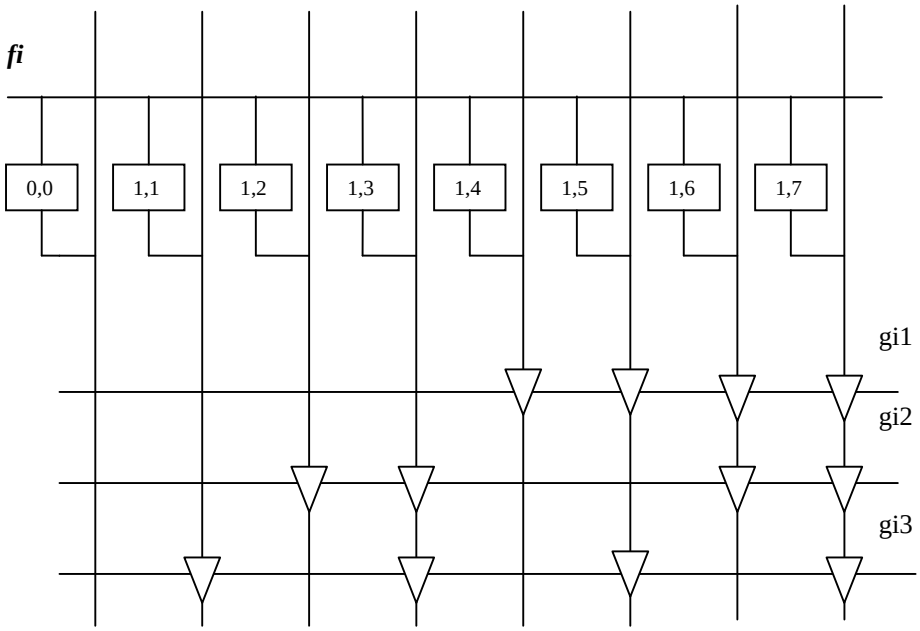

Fig. 5. Structure of translator ***T(8/2)*** with one input pin, three output pins

The parametr ***A*** of each gate ***GATE(A,j)*** from ***M(AND)*** is equal to ***K-1*** (in our case ***A=7***) and the parametrs ***j*** must be turn by the ***K-PLA*** – programmer with the help of the matrix for turning (Fig. 7, Fig. 9). The parametr ***j*** of each gate ***GATE(A,j)*** from ***M(OR)*** is equal to ***K-1*** (in our case ***j=7***) and the parametrs ***A*** must be turn by the ***K-PLA*** – programmer with the help of the matrix for turning (Fig. 7, Fig. 9).

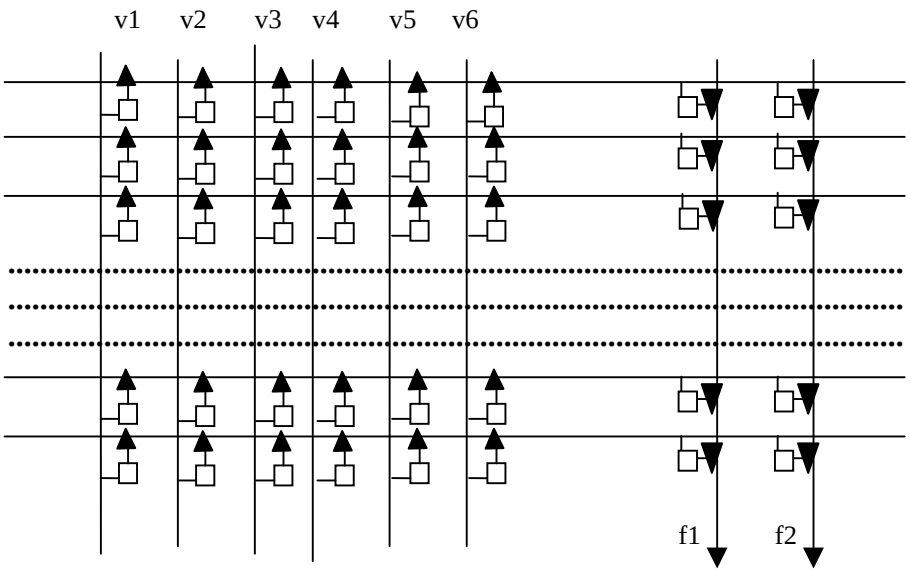

Fig. 6. Structure of ***8-PLA(6,2,20)***

For effective synthesis of ***8-PLA*** we can minimize the obtained ***8 –*** valued logical functions (Fig. 2).

Using our tools [7], we have the results of the minimization - system's intervals for the system ***(6,2,20).*** The corresponding SOP-system is showed in [7].

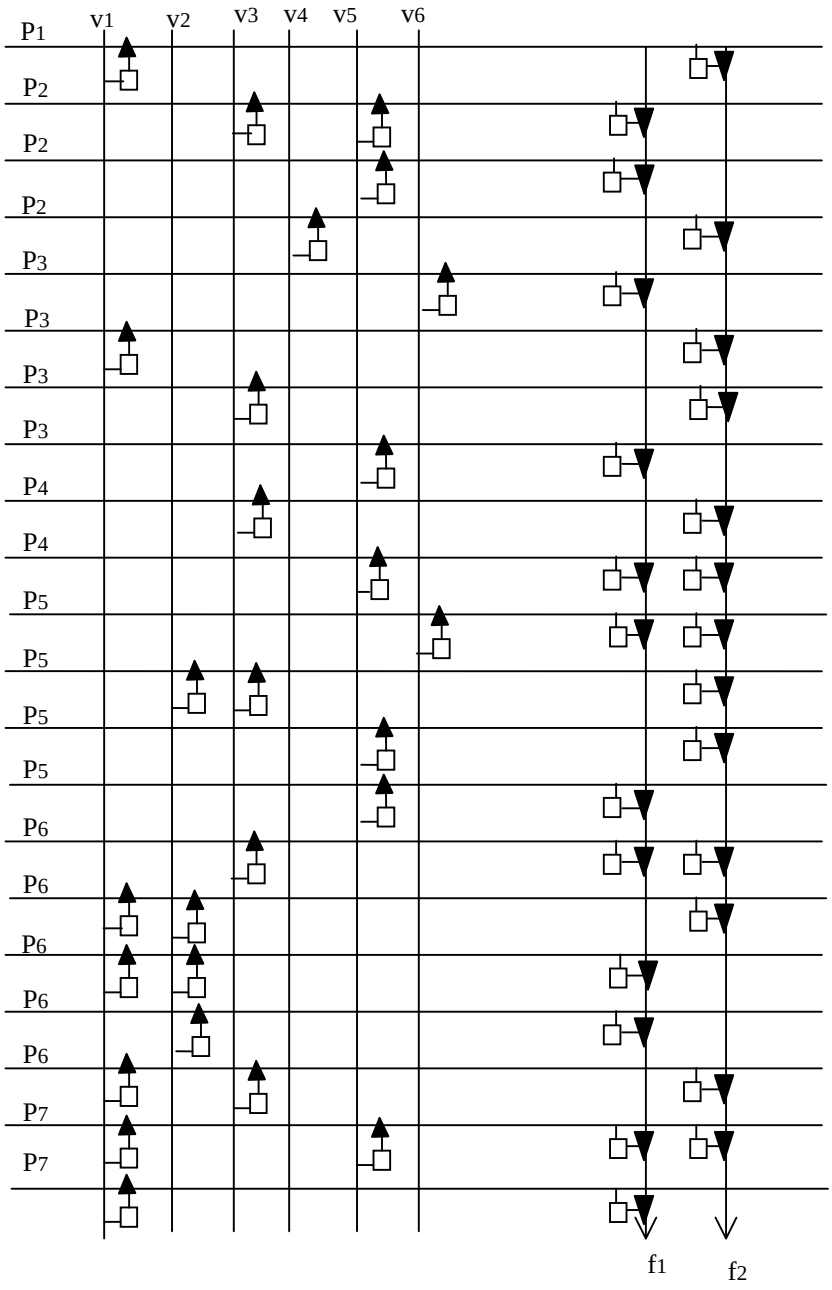

Fig. 8. Structure of ***8-PLA*** for realization ***(6,2,21)***

SOP-system is easily to realize by ***8-PLA(6,2,21)***. In our case we have the circuit, where the structure of ***8-PLA(6,2,21)*** is showed on Fig. 8 and the matrix for turning is showed on Fig. 9.

At last we have the circuit for realization our system of Boolean funtions ***(18,6,20).*** Our circuit ***S*** is showed on Fig. 10 .

Our method of synthesis [7] and new many-valued elements ***T(2/K), T(K/2)*** and ***K-PLA*** allow considerably to reduce the chip-area, which is needed for realization the system of partial Boolean functions ***(m,r,q)***.

We will estimate the effect (chip-area minimization) of the using of our method with ***K=4.***

	v1 v6		f1 f2
	430634		34
	427445		66
	754322		23
	044347		06
	545305		55
	434623		21
	026471		25
	461560		55
	064711		66
M(AND) =	761065	***M(OR)*** =	77
	426722		05
	434664		35
	061513		64
	434147		01
	706607		33
	730664		77
	434711		44
	116207		73
	471107		61
	544706		32

Fig.7

	v1 v6		f1 f2
	488888		81
	884828		28
	888878		28
	888788		82
	888884		38
	788888		83
	886888		83
	888808		38
	880888		84
M(AND) =	888818	***M(OR)*** =	44
	888885		55
	826888		85
	888868		85
	888808		58
	887888		66
	048888		86
	068888		68
	878888		68
	084888		86
	788868		77
	188888		78

Fig.9

Fig. 7. Matrix for turning ***8-PLA(6,2,20)*** (without minimization)
Fig. 9. Matrix for turning ***8-PLA(6,2,21)*** (with minimization)

The use of traditional ***2-PLA(m,r,q)*** allows to realize any system of partial Boolean functions ***(m,r,q)*** by a circuit with ***L(m,r,q)*** commutation points between input/output pins and intermediate lines, where

$$L(m,r,q) = (2m + r)*q \text{ .} \quad (1)$$

The use of our method of the synthesis with elements ***T(2/4), T(4/2)*** and ***4-PLA(m/2,r/2,q)*** allows to realize the same system of partial Boolean functions ***(m,r,q)*** by an other circuit ***S***, where the chip-area is equal to

$$L_s(m,r,q) = \frac{m}{2}(20+q) + \frac{r}{2}(12+q) \cdot \quad (2)$$

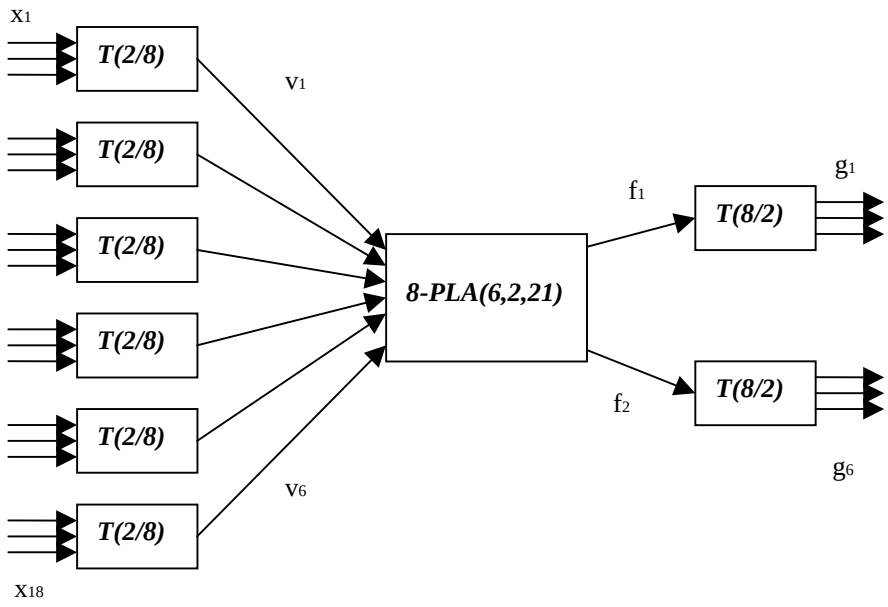

Fig. 10. The circuit for realization ***(18,6,20)***

The formula (2) was obtained from [7] by the assumption: parameters of ***m*** and ***r*** are even numbers. This assumption limits not the domain of using our method, because parameters ***m,r,q*** of "industrial" PLA are even numbers always.

We define the effect as

$$c(m,r,q) = L(m,r,q) - L_s(m,r,q) = (2m + r)* q -$$
$$-\left(\frac{m}{2}(20+q)+\frac{r}{2}(12+q)\right) = mq + q(m + r) - \frac{q}{2}(m+r) - 10m - 6r =$$
$$= mq + \frac{q}{2}(m+r) - 10m - 6r = \frac{2mq+mq+rq-20m-12r}{2} =$$
$$= \frac{q(3m+r)-12(3m+r)+16m}{2} = \frac{(3m+r)*(q-12)+16m}{2}.$$

Like that the reducing of the chip-area for the ***2-PLA(m,r,q)*** is equal to

$$c(m,r,q) = \frac{(3m+r)*(q-12)+16m}{2}. \quad (3)$$

Now we can estimate the effect of the using of our method for a circuit's realization of any system of partial Boolean functions ***(M,R,Q)*** with $M \geq m$, $R \geq r$, $Q \geq q$.

It's known [8] (formula (4.19)), what any ***(M,R,Q)*** may be realized by a circuit in the basis ***{2-PLA(m,r,q)}*** , where the number of elements ***2-PLA(m,r,q)*** is no more than

$$\left]\frac{Q}{q}\right[\left(\right]\frac{M-m}{m-r}\left[+\right]\frac{R}{r}\left[\right). \quad (4)$$

As the use of our method allows to replace a circuit ***S*** with one ***2-PLA(m,r,q)*** by the equivalent circuit ***S*** with ***T(2/4), T(4/2)*** and ***4-PLA(m/2,r/2,q)*** and to reduce the chip-area on ***c(m,r,q)*** we have the effect for any ***(M,R,Q)***, which is equal to

$$C(M,R,Q) = \left]\frac{Q}{q}\right[\left(\right]\frac{M-m}{m-r}\left[+\right]\frac{R}{r}\left[\right)\frac{(3m+r)(q-12)+16m}{2} \quad (5)$$

Example

Let the circuit's realization of the system ***(64,64,4000)*** contains ***560*** (with the help of (4)) ***2-PLA(16,8,100)***. Then we can replace this circuit by the equivalent circuit ***S*** with ***T(2/4), T(4/2)*** and ***4-PLA(8,4,100),*** where the chip-area is smaller from (5) on ***1451520*** commutation points between input/output pins and intermediate lines.

For the realization of one ***2-PLA(16,8,100)*** is needed (1) the chip-area, which is equal to ***4000.***

Then we mark that the chip-area, which was economized by using of our method, allows to place ***362*** elements ***2-PLA(16,8,100).***

In that way our method allows to reduce nearly in three times the chip-area, which is essential for placing of the circuit's realization of the system ***(64,64,4000)*** in comparison with the method [8].

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